## *CLAIMS*

What is claimed is:

1. A semiconductor memory device comprising:

a plurality of memory cells corresponding to an address space larger than $2^n$ and smaller than $2^{(n+1)}$, where n is a positive integer;

an invalid address detecting circuit for detecting that an address signal supplied from exterior indicates an address space other than said address space; and

an invalid signal outputting circuit for outputting an invalid signal to the exterior when said invalid address detecting circuit carries out said detection.

2. A semiconductor memory device according to claim 1, comprising an output controlling circuit for outputting, when said invalid address detecting circuit carries out said detection in a read operation, a data signal read in a read operation cycle immediately preceding said read operation.

3. A semiconductor memory device according to claim 2, comprising an output circuit for receiving a read data signal from said memory cells and

continuously outputting the received data to the exterior, according to a control by the output controlling circuit when said invalid address detecting circuit carries out said detection in said read operation.

4. A semiconductor memory device according to claim 1, comprising an output controlling circuit for giving high impedance to a data output terminal when said invalid address detecting circuit carries out said detection in a read operation.

5. A semiconductor memory device comprising:

a plurality of memory cells corresponding to an address space larger than $2^n$ and smaller than $2^{(n+1)}$, where n is a positive integer;

an invalid address detecting circuit for detecting that an address signal supplied from exterior indicates an address space other than said address space; and

an output controlling circuit for outputting, when said

invalid address detecting circuit carries out said detection in a read operation, a data signal read in a read operation cycle immediately preceding said read operation.

6. A semiconductor memory device according to claim 5, comprising an output circuit for receiving a read data signal from said memory cells and

continuously outputting the received data to the exterior, according to a control by the output controlling circuit when said invalid address detecting circuit carries out said detection in said read operation.

7. A semiconductor memory device comprising:

a plurality of nonvolatile memory cells corresponding to an address space larger than $2^n$ and smaller than $2^{(n+1)}$, where n is a positive integer;

a command controlling circuit for carrying out a write or an erase operation in said memory cells in response to a command input from exterior; and

an invalid address detecting circuit for detecting that an address signal supplied from exterior as the command input indicates an address space other than said address space, wherein

the command input is invalidated when said invalid address detecting circuit carries out said detection.

8. A semiconductor memory device according to claim 7, comprising an invalid signal outputting circuit for outputting an invalid signal to the exterior when said invalid address detecting circuit carries out said detection.

9. A method of controlling a semiconductor memory device comprising a plurality of memory cells corresponding to an address space larger than $2^n$ and smaller than $2^{(n+1)}$, where n is a positive integer, said method comprising the step of

outputting an invalid signal to exterior when an address signal supplied from the exterior indicating an address space other than said address space has been detected.

10. A method of controlling a semiconductor memory device, comprising a plurality of memory cells corresponding to an address space larger than $2^n$ and smaller than $2^{(n+1)}$, where n

is a positive integer and

carrying out a write or an erase operation in said memory cells in response to a command input from exterior, said method comprising the step of

invalidating the command input when an address signal supplied from the exterior indicating an address space other than the address space has been detected.